Claims:

1. A method for clock synchronization of a plurality of wireless devices (213) that are in communication with respective nodes, wherein at least some of the respective nodes are attached to different buses, comprising the steps of:

(a) synchronizing an internal time base (step 110) of a wireless master device (210a) attached to a first bus (205) by receiving a Software Beacon Alert (216) that indicates a time of a subsequent transmission and applying the Software Beacon Alert to a first phase-lock loop circuit (225) associated with the master device (210a) to create a filtered Software Beacon Alert, wherein said first phase-lock loop circuit (225) uses a phase detector with an asymmetrical gain about zero error;

(b) receiving a timing message (step 120) transmitted from the master device (210) on the first bus (205) to a second phase-lock loop circuit (235) associated with at least one slave device (210b, 210c) attached to one of a second bus (207) and a third bus (209) respectively of a plurality of buses; and

(c) providing the timing message (step 130) from the second phase-locked loop (235) to said at least one slave device (210b, 210c) attached to said one of a second bus and a third bus before the master device (210a) receives a subsequent Software Beacon Alert message, so that the wireless master device (210a) and the at least one slave device (210b, 210c) are synchronized.

2. The method according to claim 1, wherein the timing message received in step (b) is error checked.

3. The method according to claim 2, wherein the instantaneous change in cycle time for the at least one slave device is limited to +/- one clock pulse per 1394 cycle.

4. The method according to claim 1, wherein the messages transmitted and received between the wireless master device (210a) and the at least one slave device (210b, 210c) utilize an 802.11 WLAN network.

5. The method according to claim 1, further comprising:

(d) determining whether the SBA is late or early by determining an output of the first phase lock loop circuit (225), wherein a constant value that is small relative to a predetermined value indicates that the SBA is late, whereas a relatively larger and proportional gain of the first phase lock loop circuit (225) indicates that the SBA is early.

6. A system for clock synchronization of wireless nodes, comprising:

a master device (210a) attached to a first bus (205) having means for receiving a Software Beacon Alert (216) and means for communication (214) with at least one wireless device (213), said Software Beacon Alert providing an indication of a time of a subsequent transmission;

a first phase-lock loop device (225) in communication with the master device (210a), said first phase-lock loop device (225) being unsymmetrical about zero error so that a phase detector gain is constant and relatively smaller when the Software Beacon Alert is later than an indicated subsequent transmission time, and relatively larger and proportional when the Software Beacon Alert is earlier than the indicated subsequent transmission time, said first phase locked-loop providing a filtered Software Beacon Alert message;

at least one slave device (210b, 210c) that receives the filtered Software Beacon Alert message transmitted by the master device; said at least one slave device includes means for wireless communication (214) with at least one wireless device (213); and

a second phase-lock loop device (235) that is in communication with the at least one slave device (210b,210c), said second phase-lock loop device is unsymmetrical about zero error so that a phase detector gain is constant and relatively smaller when the filtered Software Beacon Alert message is later than the indicated subsequent transmission time, and relatively larger and proportional when the Software Beacon Alert message is earlier than the indicated subsequent transmission time, so that said master device (210a) of the first bus and said at least one slave device (210b, 210c) of the second bus are synchronized.

7. The system according to claim 6, wherein the filtered Software Beacon Alert message received by the second phase-lock loop device (235) is error checked.

8. The system according to claim 7, wherein the instantaneous change in cycle time for the filtered Software Beacon Alert message of said at least one slave device (210b, 210c) is +/- one clock cycle.

9. The system according to claim 8, wherein the messages transmitted and received between a first wireless device (213) in communication with the master device (210a) and a second wireless device (215) in communication with at least one slave device (210b, 210c) utilize an 802.11 WLAN network.

10. The system according to claim 6, wherein the master device (210a) and the at least one slave device (210b, 210c) conform to the IEEE 1394 device timing

standards, and said master device (210a) and said at least one slave device (210b, 210c) are connected to respective 1394 serial buses.

11. The system according to claim 10, further comprising a plurality of IEEE 1394 serial buses, with said master device (210a) being attached to a first of the plurality of IEEE serial buses and said slave device being attached a second of the plurality of IEEE 1394 buses.

12. An apparatus for receiving a Software Beacon Alert from a wireless network and synchronizing a plurality of wireless nodes, said apparatus comprising:

means for synchronizing a Software Beacon Alert that indicates a subsequent transmission time including a phase-lock loop filter (225) that is unsymmetrical about zero error, so that a phase detection gain is constant and relatively smaller when the Software Beacon Alert (SBA) is later than the indicated subsequent transmission time, and larger and proportional when the SBA is earlier than the indicated subsequent transmission time, said means for synchronizing providing a filtered Software Beacon Alert;

a master-slave arrangement (210a, 210b, 210c,) wherein a master device (210a) transmits a filtered Software Beacon Alert to at least one slave device (210b, 210c); and wherein each of said master device 210a and at least one slave device (210b, 210c) are attached to a respective 1394 serial buses, and each of said master and the at least one slave device having wireless communication with an 802.11 capable wireless device (213); and

a second phase-lock loop filter device (235) for said at least one slave device (210b, 210c) that performs error checking.

13. The apparatus according to claim 12, wherein the second phase-lock loop filter device (235) limits an instantaneous change to +/- one clock cycle.

14. The apparatus according to claim 12, wherein the second-phase lock loop filter device (235) distributes the instantaneous change over a plurality of cycles.

15. The apparatus according to claim 12, comprising at least an additional second phase-lock loop device (235) so that each respective slave device (210b, 210c) has a respective second phase-lock loop device.

16. The apparatus according to claim 12, wherein said wireless device communicating with said master device (210a) and the at least one slave device (210b, 210c) communicate via an IEEE 802.11 protocol.

17. The apparatus according to claim 12, wherein the master device (210a) and the at least one slave device (210b, 210c) comprise computers having 1394 adapter cards to communicate with a 1394 serial bus, and 802.11 adapter cards for wireless transmission with 802.11 devices.